Placer and Router for Analog Layout

Description

Analog layout automation is one of the challenges that are facing Integrated circuit IC design, as analog layout has many functions to be performed like floorplan, placement, and routing. Also, many verification steps must be performed like design rule check DRC, layout versus schematic LVS, and parasitic extraction PEX. Many of these steps are depending on the type of the circuit's constraints like Power management, Data converters (DAC/ADC), timing circuits (PLL/CDR) and radio frequency circuits (LNA/PA/Mixers) has some systematic approaches based on these constraints so it could be automated. Automation of analog layout will lead to less design iteration and faster delivery of the blocks.

Project Activities

- Design schematic recognizer tool.
- Design current mirror and differential pair matching pattern generator.
- Design floorplan tool.
- Design basic building block placer.
- Design basic building block router.
- Design top-level routing channel estimation and top-level router.
- Test and analyze the tool versus different type of circuits and add all the required enhancements
- Build and integrate these tools to have one complete flow.

Team Size

A team of 5-6 dedicated and self-motivated Students

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